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EXAMINER
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MISLEH, JUSTIN P

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/406,979

Applicant(s)

BREHMER ET AL.

Examiner

Justin P Misleh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1 - 10, 12, 14 - 20, and 23 - 35 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16, 25 and 34 is/are allowed.
- 6) ☒ Claim(s) 1 - 10, 12, 14, 15, 17 - 20, 23, 24, 26 - 33, and 35 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date. _____  | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 17 November 2004 have been fully considered but they are not persuasive.

#### Zarnowski et al.

2. This response is in regards to amended Claims 10, 20, 29, 30 and any other claims included in Applicant's arguments traversing Zarnowski et al.

3. The Applicant argues that "Zarnowski does not disclose a sample and hold circuit or a clamp circuit;" however, Applicant immediately asserts that "all circuit for performing correlated double sampling (CDS) inherently include sample and hold elements and that the CDS 34 [Zarnowski et al., figure 2] includes a sample and hold circuit with a feedback loop 32 [Zarnowski et al., figure 2]." Thus, this issue is moot.

4. The Applicant further states, "Zarnowski simply condenses all the elements required to perform CD into a single block labeled 'CDS,' block 34 ... while the feedback 32 encloses only the differential amplifier stage 30," and then concludes that, "there is no teaching or suggestion in [Zarnowski] to include the sample and hole circuits within the feedback loop."

5. The Examiner disagrees with Applicant's interpretation of the claim language and of Zarnowski et al., as will become evident below. Amended independent Claim 10 recites therein, "an amplifier circuit having a differential input transistor pair circuit with said photo sensing node voltage as one input ... wherein the amplifier circuit is coupled to the output of the sample

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and hold circuit as a second input, to form a feedback loop.” Zarnowski et al. disclose, as shown in figure 2, an amplifier circuit including a differential input transistor pair circuit, one input, and a second input. As clearly shown in figure 2, the “negative” terminal of the amplifier circuit (30) is the one input, since that input is directly coupled to the photo sensing node voltage (14), as required in the claim language. Furthermore, as clearly shown in figure 2, the “positive” terminal of the amplifier circuit (30) is a second input, since that input directly forms the feedback loop (32), also as required by the claim language. The feedback loop (32) originates at a node that couples an output of the amplifier circuit (30) to an input of the CDS circuit (34). By virtue of said node, the CDS circuit (34) is coupled within said feedback loop (32). The CDS circuit (34) includes said input and an output (designated by the “arrow” in figure 2); hence, the input of the CDS circuit and the output of the CDS circuit are coupled to together by the actual CDS circuit (34). Therefore, the coupling of the CDS input and the CDS output also includes the coupling of the CDS output and the feedback loop, thereby coupling the amplifier circuit to the output of the sample and hold circuit, as required by the claim language.

6. In summary, the claim language “coupled,” as recited in amended independent Claims 10, 20, 29, and 30, is written broadly enough such that any element in Zarnowski et al. that is coupled to the node at which the feedback loop (32) originates, via the input of that element, also couples the output of that element to that same node.

**Dhuse et al.**

7. This response is in regards to original Claims 1 – 9 and any other claims included in Applicant’s arguments traversing Dhuse et al.

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8. The Applicant's only argument is that, "the claimed method differs from the proposed combination." The Applicant supports the argument by extracting a relationship from the specification of the present invention and inferring a relationship from the disclosure of the prior art (Dhuse et al.). However, the Applicant's argument, extraction, and inference are all irrelevant because the Applicant has not detailed how the actual claim language differs from Dhuse et al.

9. More specifically, Applicant states that, "claim 1 calls for a method including correlated double sampling performed by measuring the sampled voltage after a first pixel integration ( $V_1'$ ) and then measuring the sampled voltage again after performing the rest that precedes the next pixel integration ( $V_R'$ )." In fact Claim 1, actually calls for "wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase." As will become evident below, Dhuse et al. teach what is actually called for in Claim 1.

10. Turning to Dhuse et al., as shown in figure 6, an "integration phase" corresponds block 602, a "subsequent said reset phase" corresponds to 604, a "first time instant" corresponds to (603), and a "second time instant" corresponds to 605. Since the "first time instant" (603) occurs after the "integration phase" (602) and before the "subsequent reset phase" (604) and since the "second time instant" (605) occurs after the "subsequent reset phase" (604), it clear that the photo sensing node voltage generated in the "integration phase" (602) is followed from the "first time instant" (603) to the "second time instant" (605). Dhuse et al. clearly teach the claim language recited above.

**Meyers et al.**

11. This response is in regards to Claim 15 and any other claims included in Applicant's arguments traversing Meyers et al.

12. The Applicant argues, "Meyers does not teach or suggest the topology recited in claim 15 for the sampling circuit and the clamping circuit because the elements relied upon by the Examiner do not correspond with elements of the claim or the asserted combination Fossum and Zarnowski." Furthermore, the Applicant argues, "Meyers does not have the sample and hold and clamp circuits of the claim."

13. Initially, it is important note that the Examiner relied upon Fossum et al. in view of Zarnowski et al. in view of Xu in further view of Meyers et al. in combination, not strictly a combination of Fossum et al. in view of Zarnowski et al. Also, in response to Applicant's argument that "no other elements taught by Meyers correspond with the elements of the claims or the asserted combination o Fossum and Zarnowski," it is important to note that a prior art reference must either be in the field of Applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the Applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Meyers et al. is in the Applicant's field of endeavor.

14. Finally, Claim 15 requires "wherein said clamping circuit comprises an auto-zero amplifier having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal." Claim 15 does not specifically require "sample and hold and clamp circuits" as asserted by the Applicant.

**Remaining Arguments**

15. Claims 14 (as amended), 17, and 18 depend from Claim 10 and are unpatentable for at least same reasons Claim 10. Claims 23 and 24 depend from Claim 20 and are not allowable for at least the same reasons as Claim 23. Claims 31 – 33, and 35 depend from Claim 30 and are not allowable for at least the same reasons as Claim 30.

16. The Examiner generally accepts the Applicant's amendments to the drawings and the specification with a few exceptions as detailed below:

- Applicant's amendment to the title does not overcome the previous objection because the amended title is not clearly indicative of the invention to which the claims are directed. More specifically, the claims are directed towards an image sensor circuit including a sampling circuit for performing correlated double sampling.

- Reference sign  $V_{DD}$  is introduced and described in connection with figures 1 – 3 and is only shown in figures 4 – 6. If the introduction and description of  $V_{DD}$  was intended to pertain strictly to figures 4 – 6, then  $V_{DD}$  should be introduced and described therewith. However, based upon Applicant's arguments,  $V_{DD}$  also pertains to figures 1 – 3; therefore, at least for purposes of clarity and precision,  $V_{DD}$  should be shown in figures 1 – 3.

***Specification***

17. The title of the invention is still not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. See above response for additional details.

***Drawings***

18. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: V<sub>DD</sub> (page 12).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the Examiner does not accept the changes, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 102***

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

20. **Claims 20, 26 – 28, and 30** are rejected under 35 U.S.C. 102(e) as being anticipated by Zarnowski et al. The response to arguments concerning Claims 20 and 26 – 28, as stated above, is fully incorporated into these rejections.



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21. For **Claim 20**, Zarnowski et al. disclose, as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), an image sensor circuit having a two dimensional array (see figure 4) of light sensitive pixel circuits (90a – 90c), each pixel circuit (see figure 3) comprising a photosensitive element (80) and a reset switching element (FET 76) coupled to a light sensing node (sense node 72), a differential input transistor pair (15 and 24 of operational amplifier 30; see figures 2 and 3) having a first input (15) thereof coupled to said light sensing node (sense node 72), and an enable switching element (also FET 76) coupled to selectively block output (by means of cutting off the input using Reset/Select Control) from the differential input transistor pair (15 and 24), the image sensing circuit further comprising sampling circuitry (CDS 34) for producing output signals corresponding to light incident on each of the respective pixel circuits,

wherein said sampling circuitry (CDS 34) provides a feedback path (32) to a second input (FET 24) of said differential input transistor (15 and 24) pair of each of said pixel circuits (80), and

wherein said sampling circuitry (CDS 34) includes a sample and hold circuit (inherent) circuit having an input coupled to the output from the differential input transistor pair, and having an output coupled to the second input of said differential input transistor pair (see below for further explanation).

Zarnowski et al. disclose a sampling circuit for an image sensing circuit. More specifically, Zarnowski et al., as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), a sampling circuit (CDS 34) for an image sensor circuit having a two dimensional array (see figure 4) of light sensitive pixel circuits (90a – 90c), each pixel circuit

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(see figure 3) comprising a photosensitive element (80) and an amplifier (30) wherein the amplifier (30) comprises a differential input transistor pair (15 and 24 of operational amplifier 30; see figures 2 and 3). The image sensing circuit further comprising sampling circuitry (CDS 34) for producing output signals corresponding to light incident on each of the respective pixel circuits. Furthermore, Zarnowski et al. shows in figure 2 and states, “a feedback path 32 is connects the output of the amplifier 30 to ... the gate of FET 24” and that “the output of the ... amplifier is connected to a Correlated Double Sampler which is utilized to eliminate any fixed pattern noise in the video.” Therefore, the amplifier is coupled to the output of the sample and hold circuit as a second input, to form a feedback loop.

According to Zarnowski et al., as stated in column 6 (lines 55 – 57), “selection and reset of a sense node 72 is controlled by an FET 76. Furthermore, all Correlated Double Sampling (CDS 34) circuits inherently include sample and hold circuitry within, regardless of whether it is explicitly stated.

In summary, the CDS circuit (34) includes said input and an output (designated by the “arrow” in figure 2); hence, the input of the CDS circuit and the output of the CDS circuit are coupled to together by the actual CDS circuit (34). Therefore, the coupling of the CDS input and the CDS output also includes the coupling of the CDS output and the feedback loop, thereby coupling the amplifier circuit to the output of the sample and hold circuit, as required by the claim language. The claim language “coupled” is written broadly enough such that any element in Zarnowski et al. that is coupled to the node at which the feedback loop (32) originates, via the input of that element, also couples the output of that element to that same node.

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22. As for **Claim 26**, Zarnowski et al. disclose, as shown in figures 2 – 4 and as stated in column 7 (lines 51 – 55), an image sensor circuit as claimed in Claim 20, wherein the image sensor array is implemented with CMOS technology.

23. As for **Claim 27**, Zarnowski et al. disclose, as shown in figure 2 and as stated in column 6 (lines 25 – 27), an image sensor array as claimed in Claim 20, wherein the photosensitive element comprises a photo-diode (12).

24. As for **Claim 28**, Zarnowski et al. disclose, as shown in figure 2 and as stated in column 6 (lines 25 – 27), an image sensor array as claimed in Claim 20, wherein the photosensitive element comprises a photo-gate transistor (12).

25. For **Claim 30**, Zarnowski et al. disclose, as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), a sampling circuit (34) for an image sensing circuit (figure 4) having a photosensitive element (80) which develops a photo sensing node voltage according to incident light, the sampling circuit (34) comprising:

a feedback loop (32) amplifier circuit (30) having said photo sensing node voltage as one input (14); and a sample and hold circuit having an output coupled to a second input of the feedback loop amplifier circuit, to form a feedback loop (see below for further explanation);

a clamping circuit (34) coupled to an output from the sample and hold circuit and which produces an output signal representing a double correlated sample voltage difference at said photo sensing node (see column 6, lines 38 – 39).

Zarnowski et al. disclose a sampling circuit for an image sensing circuit. More specifically, Zarnowski et al., as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), a sampling circuit (CDS 34) for an image sensor circuit having a two

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dimensional array (see figure 4) of light sensitive pixel circuits (90a – 90c), each pixel circuit (see figure 3) comprising a photosensitive element (80) and an amplifier (30) wherein the amplifier (30) comprises a differential input transistor pair (15 and 24 of operational amplifier 30; see figures 2 and 3). The image sensing circuit further comprising sampling circuitry (CDS 34) for producing output signals corresponding to light incident on each of the respective pixel circuits. Furthermore, Zarnowski et al. shows in figure 2 and states, “a feedback path 32 is connects the output of the amplifier 30 to ... the gate of FET 24” and that “the output of the ... amplifier is connected to a Correlated Double Sampler which is utilized to eliminate any fixed pattern noise in the video.” Therefore, the amplifier is coupled to the output of the sample and hold circuit as a second input, to form a feedback loop.

In summary, the CDS circuit (34) includes said input and an output (designated by the “arrow” in figure 2); hence, the input of the CDS circuit and the output of the CDS circuit are coupled to together by the actual CDS circuit (34). Therefore, the coupling of the CDS input and the CDS output also includes the coupling of the CDS output and the feedback loop, thereby coupling the amplifier circuit to the output of the sample and hold circuit, as required by the claim language. The claim language “coupled” is written broadly enough such that any element in Zarnowski et al. that is coupled to the node at which the feedback loop (32) originates, via the input of that element, also couples the output of that element to that same node.

### ***Claim Rejections - 35 USC § 103***

26. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

27. **Claims 1 – 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. in view of Dhuse et al. The response to arguments concerning Claims 1 – 9, as stated above, is fully incorporated into these rejections.

28. For **Claim 1**, Fossum et al. disclose, as shown in figures 1, 5A, 5B, and 6 and as stated in columns 2 (lines 65 – 67), 3 (lines 1 – 44), 5 (lines 27 – 67), and 6 (lines 39 – 59), a method for obtaining an output signal from a light sensing circuit (PIXEL; see figure 5A) wherein operation of the light sensing circuit (PIXEL; see figure 5A) includes a reset phase during which a photo sensing node of the light sensing circuit is charged to a reference voltage (see figure 6 and column 5, lines 45 – 54) and an integration phase during which voltage at the photo sensing node is modified by a photocurrent according to incident light intensity (see figure 6 and column 5, lines 38 – 41), the method comprising: correlated double sampling of the photo sensing node voltage to obtain an output signal representative of a change in voltage at the photo sensing node over the time of said integration phase (see column 3, lines 37 – 44); and holding said output signal for processing (by means of  $V_{LNS2}$ ); wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring before the beginning of a said integration phase and after instigation of previous said reset phase, to a second time instant occurring after completion of said integration phase. However, Fossum et al. do not disclose wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before

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instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase.

On the other hand, Dhuse et al. also disclose a method for obtaining an output signal from a light sensing circuit including correlated double sampling. More specifically, Dhuse et al. teach, as shown in figure 6 and as stated in columns 7 (lines 48 – 67) and 8 (lines 1 – 3), wherein the correlated double sampling comprises following the photo sensing node voltage from a first time instant occurring after completion (603) of a said integration phase (602) and before instigation of a subsequent said reset phase (604), to a second time instant occurring after completion of said subsequent reset phase (605). As stated in column 2 (lines 17 – 29), at the time the invention was made, one with ordinary skill in the art would have been motivated to include correlated double sampling comprising following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase, as taught by Dhuse et al., in the method of obtaining an output signal from a light sensing circuit, disclosed by Fossum et al., as a means to eliminate the noise which is generated by the reset of light sensing circuit. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to include correlated double sampling comprising following the photo sensing node voltage from a first time instant occurring after completion of a said integration phase and before instigation of a subsequent said reset phase, to a second time instant occurring after completion of said subsequent reset phase, as taught by Dhuse et al., in the method of obtaining an output signal from a light sensing circuit, disclosed by Fossum et al.

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29. As for **Claim 2**, it is important to note that it is an intrinsic characteristic of CMOS transistor to exhibit clock feed-through, thus, feed-through is present with Fossum et al. Furthermore, Fossum et al. disclose, as shown in figures 5A and 6 and as stated in column 5 (lines 45 – 54), wherein said reset phase comprises charging said photo sensing node to said reference voltage by turning on and off a reset transistor (530) coupled to the photo sensing node such that, after turning off the reset transistor, a feed through effect at the reset transistor causes a reduction in voltage at the photo sensing node before instigation of the subsequent reset phase, and, according to Dhuse et al., wherein the second time instant (605; see figure 6) of said correlated double sampling is after said photo sensing node voltage reduction due to feed through effect.

30. As for **Claim 3**, Fossum et al. disclose, as shown in figures 1, 5A, 5B, and 6 and as stated in columns 2 (lines 65 – 67), 3 (lines 1 – 44), 5 (lines 27 – 67), and 6 (lines 39 – 59), wherein a sample and hold circuit (516 and 526) is coupled receive signals representing the photo sensing node voltage, and a clamping circuit (550 and 552) is coupled to the sample and hold circuit, and wherein said correlated double sampling and said holding of the output signal is accomplished by manipulation of input signals (SHS, SHR, and CLAMP) to said sample and hold circuit and said clamping circuit.

31. As for **Claim 4**, Fossum et al. disclose, as stated in column 5 (lines 9 – 12), wherein said light sensing circuit includes a photo-diode coupled to said photo sensing node, and wherein said photocurrent flows through the photo-diode according to the intensity of light incident thereon.

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32. As for **Claim 5**, Fossum et al. disclose, as stated in column 5 (lines 9 – 12), wherein said light sensing circuit includes a photo-gate transistor coupled to said photo sensing node and through which said photo-current flows according to the intensity of light incident thereon.

33. As for **Claim 6**, Fossum et al. disclose, as shown in figures 5B and 6 and as stated in columns 5 (lines 54 – 60) and 7 (lines 17 – 37), wherein said integration phase and said reset phase are performed in an alternating cycle, and wherein an output signal is obtained for said light sensing circuit following each cycle.

34. As for **Claim 7**, Fossum et al. disclose, as stated in column 5 (lines 27 – 35), wherein a plurality of said light sensing circuits are arranged in a two dimensional image sensing array, and wherein an output signal is obtained for each of said light sensing elements in the array following each said cycle, so as to obtain two dimensional image data.

35. As for **Claim 8**, Fossum et al. disclose, as shown in figures 5A and 5B, wherein a sample and hold circuit (516 and 526) is coupled to selectively receive signals representing the photo sensing node voltage from a plurality of light sensing circuits in said array (see column 5, lines 54 – 60), and a clamping circuit (550 and 552) is coupled to the sample and hold circuit (516 and 526), and wherein said correlated double sampling and said holding of the output signal is accomplished by manipulation of input signals (SHS, SHR, and CLAMP) to said sample and hold circuit and said clamping circuit.

36. As for **Claim 9**, Fossum et al. disclose, as shown in figures 1, 5A, 5B, and 6 and as stated in columns 2 (lines 65 – 67), 3 (lines 1 – 44), 5 (lines 27 – 67), and 6 (lines 39 – 59), wherein said light sensing circuit (see figure 5A and 5B), said sample and hold circuit (516 and 526) and



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said clamping circuit are all fabricated on the same silicon substrate using a CMOS integrated circuit technology (see column 5, lines 27 – 35).

37. **Claims 10, 17, 19, and 29** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. in view of Zarnowski et al. The response to arguments concerning Claims 10, 17, 19, and 29, as stated above, is fully incorporated into these rejections.

38. For **Claim 10**, Fossum et al. disclose, as shown in figures 1, 5A, 5B, and 6 and as stated in columns 2 (lines 65 – 67), 3 (lines 1 – 44), 5 (lines 27 – 67), and 6 (lines 39 – 59), a sampling circuit (comprised of both the column circuit 155 and the pixel circuit 150) for an image sensing circuit (pixel circuit 150) having a photosensitive element (100/502) which develops a photo sensing node voltage according to incident light, the sampling circuit (155/150) comprising:

an amplifier circuit (508) having said photo sensing node voltage as one input (as the gate of amplifier 508);

a sample and hold circuit (516 and 526) coupled to an output of the amplifier circuit (508; see figure 5A), and a clamping circuit (550 and 552) coupled to an output of the sample and hold circuit (516 and 526; see figure 5B) and produce an output signal representing a double correlated sample voltage difference at said photo sensing node (see column 3, lines 37 – 44).

While Fossum et al. disclose a sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising an amplifier circuit having said photo sensing node voltage as input; wherein the amplifier circuit comprises a source follower circuit; Fossum et al. do not disclose wherein the amplifier circuit comprises a differential input transistor pair circuit and

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wherein the amplifier circuit is coupled to the output of the sample and hold circuit as a second input, to form a feedback loop.

On the other hand, Zarnowski et al. also disclose a sampling circuit for an image sensing circuit. More specifically, Zarnowski et al., as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), a sampling circuit (CDS 34) for an image sensor circuit having a two dimensional array (see figure 4) of light sensitive pixel circuits (90a – 90c), each pixel circuit (see figure 3) comprising a photosensitive element (80) and an amplifier (30) wherein the amplifier (30) comprises a differential input transistor pair (15 and 24 of operational amplifier 30; see figures 2 and 3). The image sensing circuit further comprising sampling circuitry (CDS 34) for producing output signals corresponding to light incident on each of the respective pixel circuits. Furthermore, Zarnowski et al. shows in figure 2 and states, “a feedback path 32 is connects the output of the amplifier 30 to ... the gate of FET 24” and that “the output of the ... amplifier is connected to a Correlated Double Sampler which is utilized to eliminate any fixed pattern noise in the video.” Therefore, the amplifier is coupled to the output of the sample and hold circuit as a second input, to form a feedback loop.

In summary, the CDS circuit (34) includes said input and an output (designated by the “arrow” in figure 2); hence, the input of the CDS circuit and the output of the CDS circuit are coupled to together by the actual CDS circuit (34). Therefore, the coupling of the CDS input and the CDS output also includes the coupling of the CDS output and the feedback loop, thereby coupling the amplifier circuit to the output of the sample and hold circuit, as required by the claim language. The claim language “coupled” is written broadly enough such that any element

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in Zarnowski et al. that is coupled to the node at which the feedback loop (32) originates, via the input of that element, also couples the output of that element to that same node.

As stated in columns 3 (lines 8 – 10 and 21 – 24), 4 (lines 1 – 3 and 19 – 21), and 6 (lines 35 and 36) of Zarnowski et al., at the time the invention was made it would have been obvious to one with ordinary skill in the art include an amplifier wherein the amplifier comprises a differential input transistor pair circuit wherein the amplifier circuit is coupled to the output of the sample and hold circuit, as taught by Zarnowski et al., in the sampling circuit for an image sensing circuit, disclosed by Fossum et al., for the advantage of enabling high speed high quality video readout with an increased maximum pixel rate, reduced fixed pattern noises, reduced system size, reduced complexity, and elimination of amplifier gain variability.

39. As for **Claim 17**, Fossum et al. in view of Zarnowski et al. teach wherein a plurality of image sensing circuits are arranged in an array, each forming a pixel circuit of an image sensor, and wherein each pixel circuit includes a said photo sensitive element (80; Fossum et al.), a reset switching element (530; Fossum et al.) and a said differential input transistor pair as part of said amplifier circuit (30; Zarnowski et al.), and wherein the sample and hold circuit (COLUMN; Fossum et al.) and the clamping circuit (Figure 5B; Fossum et al.) are shared by a plurality of pixel circuits in the image sensor array (see Figures 1, 5A, and 5B; Fossum et al.).

40. As for **Claim 19**, Fossum et al. disclose, as stated in the abstract and in column 5 (lines 33 – 35), a sampling circuit (comprised of both the column circuit 155 and the pixel circuit 150) as claimed in Claim 10, wherein the image sensing circuit (pixel circuit 150), amplifier circuit (508), sample and hold circuit (516 and 526) and clamping circuit (550 and 552) are constructed in the same integrated circuit using CMOS fabrication technology.

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41. For **Claim 29**, Fossum et al. disclose, as shown in figures 1, 5A, 5B, and 6 and as stated in columns 2 (lines 65 – 67), 3 (lines 1 – 44), 5 (lines 27 – 67), and 6 (lines 39 – 59), in an image sensor circuit (see figures 5A and 5B) having an array of pixels including light sensing nodes at each of which a change in voltage can be imparted by exposure to a light source, a method for obtaining output signals representing the voltage changes at the light sensing nodes in order to obtain image data, comprising:

at each said pixel (PIXEL; see figure 5A) providing an amplifier circuit (508) with an input driven by the voltage on the respective light sensing node to produce an amplifier output;

providing a sample and hold circuit (COLUMN; see figure 5A) coupled to selectively (by means of ROW select switch 514) receive the amplifier output of a said pixel amplifier circuit in the array, the sample and hold circuit (COLUMN) being controlled by a first control signal input (comprised of both control signals SHS and SHR) and producing an output signal (A and B; see figure 5A);

providing a clamping circuit (see figure 5B) coupled to the sample and hold circuit output (by means of A and B; see figures 5A and 5B), the clamping circuit (see figure 5B) producing an output (VS/VR OUT; see figure 5B) according to the received sample and hold signal input and a second control signal (provided at the gate of Clamp switches 550 and 552); and

controlling the first and second control signals to the sample and hold circuit and the clamping circuit respectively so as to perform correlated double sampling of the voltage at the respective light sensing node so as to obtain a representation of the change of voltage thereat imparted substantially only by exposure to light (see column 3, lines 37 – 44).

While Fossum et al. disclose a sampling circuit for an image sensing circuit having a photosensitive element which develops a photo sensing node voltage according to incident light, the sampling circuit comprising an amplifier circuit having said photo sensing node voltage as input; wherein the amplifier circuit comprises a source follower circuit; Fossum et al. do not disclose wherein the amplifier circuit comprises a differential amplifier and wherein the amplifier circuit is coupled to the sample and hold circuit within a feedback loop.

On the other hand, Zarnowski et al. also disclose a sampling circuit for an image sensing circuit. More specifically, Zarnowski et al., as shown in figures 2 – 4 and as stated in columns 6 (lines 21 – 67) and 7 (lines 1 – 41), a sampling circuit (CDS 34) for an image sensor circuit having a two dimensional array (see figure 4) of light sensitive pixel circuits (90a – 90c), each pixel circuit (see figure 3) comprising a photosensitive element (80) and an amplifier (30) wherein the amplifier (30) comprises a differential amplifier (15 and 24 of operational amplifier 30; see figures 2 and 3). The image sensing circuit further comprising sampling circuitry (CDS 34) for producing output signals corresponding to light incident on each of the respective pixel circuits. Furthermore, Zarnowski et al. shows in figure 2 and states, “a feedback path 32 is connects the output of the amplifier 30 to ... the gate of FET 24” and that “the output of the ... amplifier is connected to a Correlated Double Sampler which is utilized to eliminate any fixed pattern noise in the video.” Therefore, the amplifier is coupled to the sample and hold circuit within a feedback loop.

The claim language “coupled” is written broadly enough such that any element in Zarnowski et al. that is coupled to the node at which the feedback loop (32) originates, via the input of that element, also couples the output of that element to that same node.

As stated in columns 3 (lines 8 – 10 and 21 – 24), 4 (lines 1 – 3 and 19 – 21), and 6 (lines 35 and 36) of Zarnowski et al., at the time the invention was made it would have been obvious to one with ordinary skill in the art include an amplifier wherein the amplifier comprises a differential amplifier wherein the amplifier circuit is coupled to the sample and hold circuit within a feedback loop, as taught by Zarnowski et al., in the sampling circuit for an image sensing circuit, disclosed by Fossum et al., for the advantage of enabling high speed high quality video readout with an increased maximum pixel rate, reduced fixed pattern noises, reduced system size, reduced complexity, and elimination of amplifier gain variability.

42. **Claims 14 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. in view of Zarnowski et al. in further view of Xu.

43. As for **Claim 14**, Fossum et al. disclose a sampling circuit (comprised of both the column circuit 155 and the pixel circuit 150) for an image sensing circuit, the sampling circuit (155/150) comprising: an amplifier circuit (508) having said photo sensing node voltage as input (as the gate of amplifier 508); a sample and hold circuit (516 and 526) coupled to receive an output of the amplifier circuit (508; see figure 5A), and a clamping circuit (550 and 552) coupled to receive an output of the sample and hold circuit (516 and 526; see figure 5B) and produce an output signal representing a double correlated sample voltage difference at said photo sensing node (see column 3, lines 37 – 44). Furthermore, Zarnowski et al. teach wherein the amplifier (30) comprises a differential input transistor pair (15 and 24 of operational amplifier 30; see figures 2 and 3), wherein a feedback path (32) exists between an output of the amplifier (30) and

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an input of the amplifier (30), and wherein the sampling circuit is coupled within the feedback loop.

However, Fossum et al. in view of Zarnowski et al. do not disclose wherein a source follower circuit coupled within said feedback loop is used to couple the output of the sample and hold circuit to said clamping circuit.

On the other hand, Xu also discloses an image sensor circuit comprising sampling circuitry. More specifically, Xu discloses, as shown in figures 1 and 2 and as stated in columns 2 (lines 40 – 67), 3 (lines 1 – 7), 4 (lines 12 – 57), an image sensor circuit (see figure 1) comprising sampling circuitry (10) wherein the sampling circuitry (10) further includes a source follower circuit (linear gain amplifiers 41 and 42) which provides an input to a clamping circuit (clamping circuit 21 and 22). As stated in column 1 (lines 48 – 52), at the time invention was made, one with ordinary skill in the art would have been motivated to include sampling circuitry wherein the sampling circuitry further includes a source follower circuit which provides an input to a clamping circuit, as taught by Xu, in the image sensor circuit, disclosed by Fossum et al. in view of Zarnowski et al., as a means to provide sampling circuitry that requires a small chip area and less power. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a source follower circuit which provides an input to a clamping circuit, as taught by Xu, in the image sensor circuit, disclosed by Fossum et al. in view of Zarnowski et al.

44. As for **Claim 18**, Zarnowski et al. disclose, as stated in column 6 (lines 33 – 39), wherein the feedback (32) loop is arranged so that the amplifier circuit has a gain of greater than unity. More specifically, Zarnowski et al. states, “the amplifier circuit 30 is configured as a positive

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feedback unity gain amplifier ... the amplifier 30 could be configured to have gain, a full differential input or any operational amplifier configuration as the application required.”

45. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Fossum et al. in view of Zarnowski et al. in view of Xu in further view of Meyers.

46. As for **Claim 15**, Fossum et al. in view of Zarnowski et al. in view of Xu teach in combination a sampling circuit comprising an amplifier circuit, a sample and hold circuit coupled to receive an output of the amplifier circuit, and a clamping circuit coupled to receive an output of the sample and hold circuit and produce an output signal representing a double correlated sample voltage difference, wherein a feedback path exists between an output of the amplifier and an input of the amplifier, and wherein the sampling circuit is coupled within the feedback loop, wherein a source follower circuit coupled within said feedback loop is used to couple the output of the sample and hold circuit to said clamping circuit.

However, Fossum et al. in view of Zarnowski et al. in view of Xu do not teach wherein the clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

On the other hand, Meyers also discloses a sampling circuit comprising a sample and hold circuit and a clamping circuit. More specifically, as shown in figure 6 and as stated in column 11 (lines 38 – 63), Meyers discloses a sampling circuit (40) comprising a sample and hold circuit (42 and 44) and a clamping circuit (46 and associated circuitry), wherein the clamping circuit (46 and associated circuitry) comprises an auto-zero amplifier circuit (46)



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having a feedback loop which includes a first capacitive storage element (see figure 6) coupled in parallel with a switching element (see figure 6) controlled by a clamp signal (RESET). As stated in column 11 (lines 60 – 63), at the time the invention was made, one with ordinary skill in the art would have been motivated to include a clamping circuit comprising an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, as taught by Meyers, in the sampling circuit, taught by Fossum et al. in view of Zarnowski et al. in view of Xu, as a means to provide correlated double sampling capable of reducing Johnson noise, flicker noise, KTC noise, and 1/f noise in a single integration period. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a clamping circuit comprising an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, as taught by Meyers, in the sampling circuit, taught by Fossum et al. in view of Zarnowski et al. in view of Xu.

47. **Claims 23, 31, and 35** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarnowski et al. in view of Xu.

48. As for **Claims 23 and 31**, Zarnowski et al. disclose, as shown in figure 2 and as stated in column 6 (lines 29 – 39), sampling circuitry (CDS 34) connected to the output of the amplifier (30), wherein a feedback path (32) connects the output of the amplifier (30) to the gate of FET (24); hence, the sampling circuitry (CDS 34) is coupled within the feedback path (32). However,

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Zarnowski et al. do not disclose wherein the sampling circuitry further includes a source follower circuit coupled within said feedback path which provides an input to a clamping circuit.

On the other hand, Xu also discloses an image sensor circuit comprising sampling circuitry. More specifically, Xu discloses, as shown in figures 1 and 2 and as stated in columns 2 (lines 40 – 67), 3 (lines 1 – 7), 4 (lines 12 – 57), an image sensor circuit (see figure 1) comprising sampling circuitry (10) wherein the sampling circuitry (10) further includes a source follower circuit (linear gain amplifiers 41 and 42) which provides an input to a clamping circuit (clamping circuit 21 and 22). As stated in column 1 (lines 48 – 52), at the time invention was made, one with ordinary skill in the art would have been motivated to include sampling circuitry wherein the sampling circuitry further includes a source follower circuit which provides an input to a clamping circuit, as taught by Xu, in the image sensor circuit, disclosed by Zarnowski et al., as a means to provide sampling circuitry that requires a small chip area and less power. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a source follower circuit which provides an input to a clamping circuit, as taught by Xu, in the image sensor circuit, disclosed by Zarnowski et al.

49. As for **Claim 35**, Zarnowski et al. disclose, as stated in column 6 (lines 33 – 39), wherein the feedback (32) to the differential input transistor pair is arranged so that the amplifier circuit has a gain of greater than unity. More specifically, Zarnowski et al. states, “the amplifier circuit 30 is configured as a positive feedback unity gain amplifier ... the amplifier 30 could be configured to have gain, a full differential input or any operational amplifier configuration as the application required.”

50. **Claim 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarnowski et al. in view of Xu in further view of Wayne.

51. As for **Claim 24**, while Zarnowski et al. in view of Xu teach an image sensor circuit comprising sampling circuitry for producing output signals corresponding to light incident on each of the respective pixel circuits, wherein said sampling circuitry provides a feedback path to a second input of said differential input transistor pair of each of said pixel circuits wherein said sampling circuitry includes a sample and hold circuit coupled within said feedback path, wherein the sampling circuitry further includes a source follower circuit coupled within said feedback path which provides an input to a clamping circuit. However, Zarnowski et al. in view of Xu do not disclose wherein said clamping circuit comprises an auto-zero amplifier circuit.

On the other hand, Wayne also discloses an image sensor circuit comprising sampling circuitry including a clamping circuit. More specifically, Wayne discloses, as shown in figure 2 and as stated in columns 4 (lines 54 – 67) and 5 (lines 1 – 26), an image sensor circuit (25) comprising sampling circuitry (30) including a clamping circuit ( $T_7$ ,  $C_2$ ,  $T_9$ , and  $T_{10}$ ).

Furthermore, Wayne discloses that the clamping circuit ( $T_7$ ,  $C_2$ ,  $T_9$ , and  $T_{10}$ ) comprises an auto-zero amplifier ( $T_9$  and  $T_{10}$ ). As stated in column 2 (lines 17 – 27), at the time the invention was made, one with ordinary skill in the art would have been motivated to include a clamping circuit comprising an auto-zero amplifier, as taught by Wayne, in the image sensor circuit comprising sampling circuitry, disclosed by Zarnowski et al. in view of Xu, as a means to provide an image sensor circuit that minimizes the effects due to device variations using a simpler, compact, high-speed implementation. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a clamping circuit comprising an

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auto-zero amplifier, as taught by Wayne, in the image sensor circuit comprising sampling circuitry, disclosed by Zarnowski et al. in view of Xu.

52. **Claim 32** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarnowski et al. in view of Wayne.

53. As for **Claim 32**, while Zarnowski et al. teach an image sensor circuit comprising sampling circuitry for producing output signals corresponding to light incident on each of the respective pixel circuits, wherein said sampling circuitry provides a feedback path to a second input of said differential input transistor pair of each of said pixel circuits wherein said sampling circuitry includes a sample and hold circuit coupled within said feedback path. However, Zarnowski et al. do not disclose wherein said clamping circuit comprises an auto-zero amplifier circuit.

On the other hand, Wayne also discloses an image sensor circuit comprising sampling circuitry including a clamping circuit. More specifically, Wayne discloses, as shown in figure 2 and as stated in columns 4 (lines 54 – 67) and 5 (lines 1 – 26), an image sensor circuit (25) comprising sampling circuitry (30) including a clamping circuit ( $T_7$ ,  $C_2$ ,  $T_9$ , and  $T_{10}$ ).

Furthermore, Wayne discloses that the clamping circuit ( $T_7$ ,  $C_2$ ,  $T_9$ , and  $T_{10}$ ) comprises an auto-zero amplifier ( $T_9$  and  $T_{10}$ ). As stated in column 2 (lines 17 – 27), at the time the invention was made, one with ordinary skill in the art would have been motivated to include a clamping circuit comprising an auto-zero amplifier, as taught by Wayne, in the image sensor circuit comprising sampling circuitry, disclosed by Zarnowski et al., as a means to provide an image sensor circuit that minimizes the effects due to device variations using a simpler, compact, high-speed

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implementation. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a clamping circuit comprising an auto-zero amplifier, as taught by Wayne, in the image sensor circuit comprising sampling circuitry, disclosed by Zarnowski et al.

54. **Claim 33** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zarnowski et al. in view of Wayne in further view of Meyers.

55. As for **Claim 33**, Zarnowski et al. in view of Wayne teach an image sensor circuit comprising sampling circuitry provides a feedback path to a second input of a differential input transistor pair of each of a plurality of pixel circuits wherein the sampling circuitry includes a sample and hold circuit coupled within said feedback path, wherein the sampling circuitry further includes a clamping circuit comprising an auto-zero amplifier.

However, Zarnowski et al. in view of Wayne do not teach wherein the clamping circuit comprises an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

On the other hand, Meyers also discloses a sampling circuit comprising a sample and hold circuit and a clamping circuit. More specifically, as shown in figure 6 and as stated in column 11 (lines 38 – 63), Meyers discloses a sampling circuit (40) comprising a sample and hold circuit (42 and 44) and a clamping circuit (46 and associated circuitry), wherein the clamping circuit (46 and associated circuitry) comprises an auto-zero amplifier circuit (46) having a feedback loop which includes a first capacitive storage element (see figure 6) coupled in parallel with a switching element (see figure 6) controlled by a clamp signal (RESET). As

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stated in column 11 (lines 60 – 63), at the time the invention was made, one with ordinary skill in the art would have been motivated to include a clamping circuit comprising an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, as taught by Meyers, in the sampling circuit, taught by Zarnowski et al. in view of Wayne, as a means to provide correlated double sampling capable of reducing Johnson noise, flicker noise, KTC noise, and 1/f noise in a single integration period. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have included a clamping circuit comprising an auto-zero amplifier circuit having a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal, as taught by Meyers, in the sampling circuit, taught by Zarnowski et al. in view of Wayne.

*Allowable Subject Matter*

56. **Claims 16, 25, and 34** are allowed. Claims 16, 25, and 34 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

57. For **Claims 16, 25, and 34**, the closest prior art teaches, in the very least, several different embodiments including a sampling circuit for an image sensing circuit having a photosensitive element, wherein the sampling circuit comprises a feedback loop amplifier circuit having an output from the photosensitive elements as input; and a clamping circuit coupled to receive an output from the feedback loop amplifier circuit and produce an output signal representing a double correlated sample voltage difference at the output, wherein said clamping

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circuit comprises an auto-zero amplifier circuit with a feedback loop which includes a first capacitive storage element coupled in parallel with a switching element controlled by a clamp signal.

However, the closest prior art does not teach or fairly suggest wherein the amplifier circuit of the clamping circuit has a first input coupled to a reference voltage and a second input coupled by way of a second capacitive element to receive said output from the feedback loop amplifier, and wherein said clamping circuit is controlled by a clamp signal such that in a first state the output of the clamping circuit amplifier is fixed by said reference voltage and in a second state the clamping circuit output changes in accordance with said feedback loop amplifier output from a baseline of the fixed reference voltage output.

### *Conclusion*

58. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

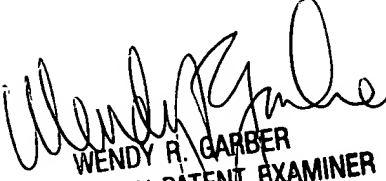
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Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090 (571.272.7313 ~ March 2005). The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:00 PM and on alternating Fridays from 8:00 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM  
February 16, 2005

  
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